Tutorial for I-V Characterization of MOSFET using Cascade Probe Station and Agilent Parameter Analyzer

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Chapter 1: I-V Characteristics of a MOSFET

1.1 Introduction:

The chip consists of 3-enhancement mode MOSFETs. Enhancement mode devices need an input voltage to create a channel between the drain and source, that is, to be 'ON'. For N channel enhancement mode MOSFET, there is a P doped substrate between the drain and the source. The drain and the source themselves are made out of N doped material. For NMOSFET to conduct, we have to apply a positive voltage at the gate. This will attract electrons and repel holes, thus forming an N channel between the drain and the source. The substrate or body is tied to the source for 2 MOSFETs on the chip and we are going to analyze just these ones.

By default, the gate, source and drain are isolated from each other by silicon dioxide insulation. Once the voltage applied at the gate is above a specific value, there is a continuous channel formed between the source and drain. This voltage is the threshold voltage of the MOSFET. With the gate voltage (Vgs) greater the threshold voltage (Vt), as the drain-source voltage is increased over 0V, current starts flowing through the drain. As this voltage is increased, the current flowing through the channel keeps increasing. After a certain value, the drain current remains constant, no matter how much you increase the voltage. As the gate voltage with respect to the drain is increased, a depletion region is formed. Although the electrons are attracted, the channel size goes on decreasing around the gate and drain. Thus as the drain voltage is increased, the current still remains the same.

1.2 Region of Operation of MOSFET:

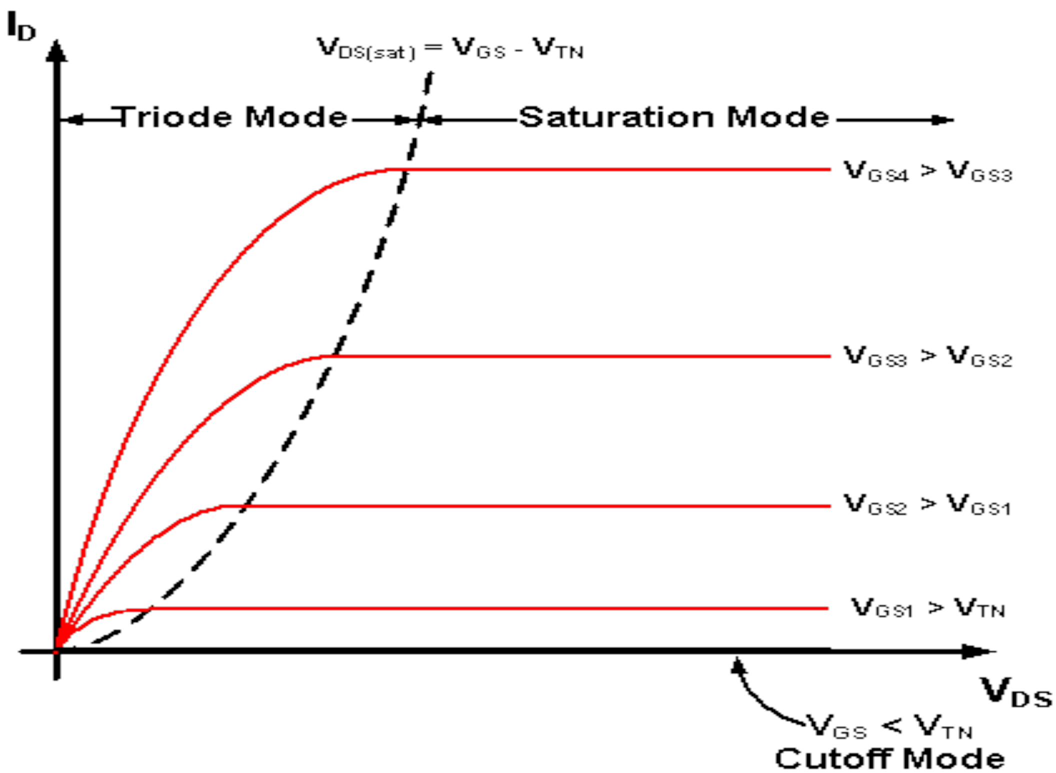


Fig 1: Regions of operation of a MOSFET

Thus we have 3 regions of operation for a MOSFET,

1. Cut-Off Region: During this period there is no channel between the drain and source. This occurs when Vds = 0 or when Vgs < Vt.

2. Linear or Triode region: During this period the channel between the source and drain has been created and occurs when Vgs > Vt and 0 < Vds < Vds (Sat), where Vds (Sat) = Vgs-Vt.

3. Saturation Region: During this period the channel is already formed, but the maximum drain current has been reached. The current remains constant irrespective of the voltage supplied. This occurs when, Vgs > Vt, and Vds > Vds (Sat)

Chapter 2: Introduction to instruments used for testing

2.1 Instruments used:

1. Probe Station: The probe station used is a Cascade micro tech 11000 series. The chip under test is going to be placed on the probe station. We will be using 3 probes, which are going to be placed on the desired pins on the chip, to verify the voltage characteristics of a MOSFET. A microscope unit is directed over the chip under test. This unit is connected to another computer. The monitor attached with this computer, shows the image of the chip. We have to place the probes looking at this monitor carefully. The air compressor is used to reduce the volume of the gas and to increase he density. This instrument is required to be ON for the floating table on which the probe station is placed to work efficiently and also for the movement of the microscope.

2. Semiconductor Parameter Analyzer: We will be using Agilent's B1500A series parameter analyzer to obtain the desired results. The parameter analyzer is capable of providing and monitoring high and low voltage/current. The Parameter Analyzer has the ability to measure extremely low currents and voltages. It also has integrated capacitance-measuring capabilities, which makes it an apt instrument for our test. It can also measure negative biased temperature instability, which is optimal for reliability measurements of MOSFETs. The analyzer we will be using has 3 types of test, Classic test, Application test and tracer test. For our analysis, we will be using Application test because it is most suitable for the voltage analysis of a MOSFET.

2.2 Instructions for Instrument usage:

Before we start with the test, these 3 instruments along with the computer on which the image from the microscope can be seen, have to be turned 'ON'.

First, the air compressor has to be turned on. Turning the knob as shown below can do this. Next, turn on the parameter by switching on the power button. Start 'Easy expert' software installed on it. There are 3 types of test modes for the parameter analyzer, namely, classic mode, application test, and tracer test. According to the requirements and the chip under test, we need to decide which type of test suits best. Application test has a ready schematic for MOSFETs, which makes it easy to analyze its voltage characteristics. Therefore, we will be using application test to test the chip.

(After, selecting application test, select CMOS, and then make your selection according to your requirement.)

Switch on the computer on which the image of the chip from the microscope will be seen. Start nucleus software from the desktop. Select the video option, which will show the image of the chip.

Before you switch on the probe station, set the chip in the desired position. According to the type of test, the chip can be positioned to make it easier for probe placement. After appropriate positioning, switch on the probe station. Next, place the probes at the required pins on the chip.

Chapter 3: The Chip under test

3.1 Introduction to the chip:

CD4007 UB chip consists of 3 n channel and 3 p channel enhancement type MOS transistors. The chip consists of 14 pins of which, pin 7 in Vss and pin 14 is Vdd. This chip provides output characteristics that are standardized symmetrically. It is tested at 20V for quiescent current. At 18V, it has a maximum input current of 1μA over full temperature range. The supply voltage range for Ta being full temperature package range is 3V to 18V, which is basically nominal operating mode. This range of supply voltage provides maximum reliability.

3.2 Functional Block diagram for CD4007UB chip:

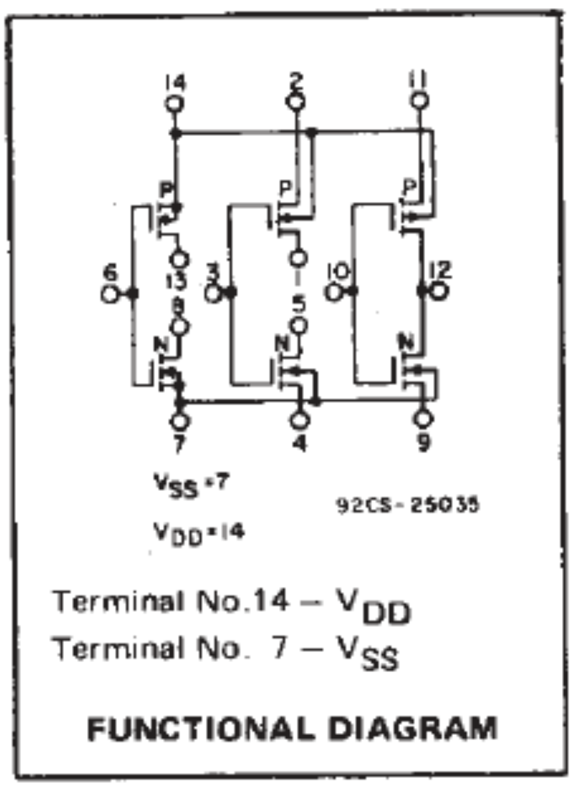


Fig 2: Functional diagram of CD4007UB

The figure above shows the functional diagram of a CD4007 UB chip. It consists of 3 inverters. For the first inverter, the body for the PMOS and NMOS are shorted to their respective sources. The drains of the PMOS and NMOS are shorted, therefore making it easy to analyze the characteristics of the individual MOSFET's, since we would have to use only 3 probes for each MOSFET. For the other 2 inverters, not only are the drains shorted but also the body for both inverters forms a separate pin, which means using 4 probes, which could mean decreasing the reliability of the test.

3.3 How to read the chip:

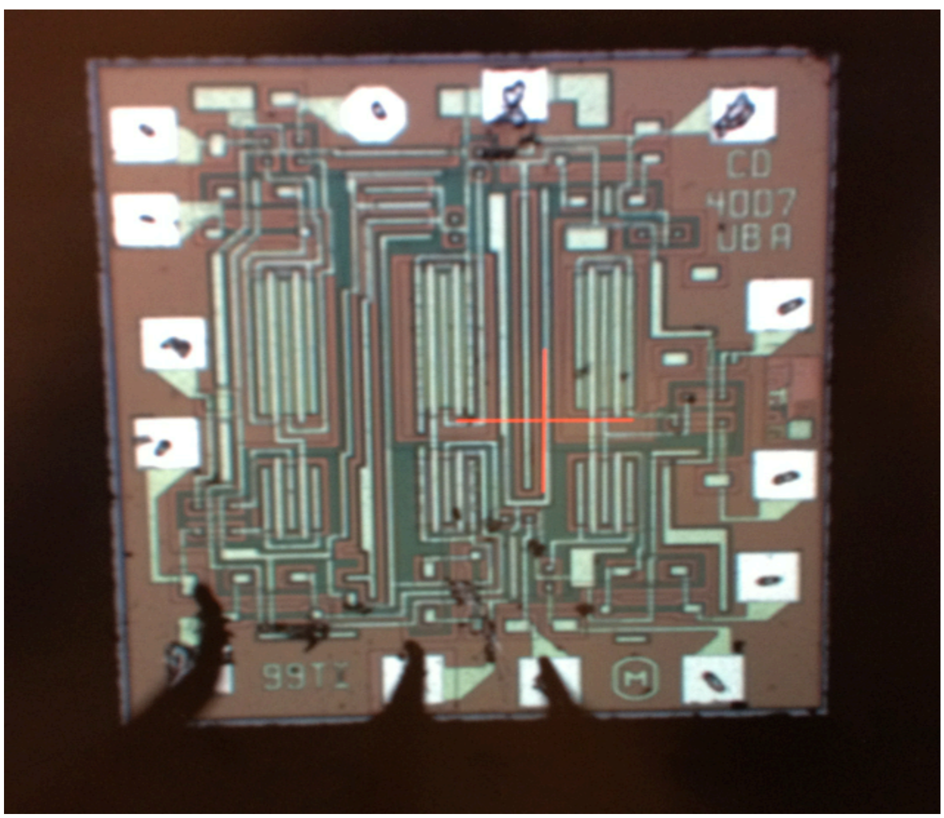
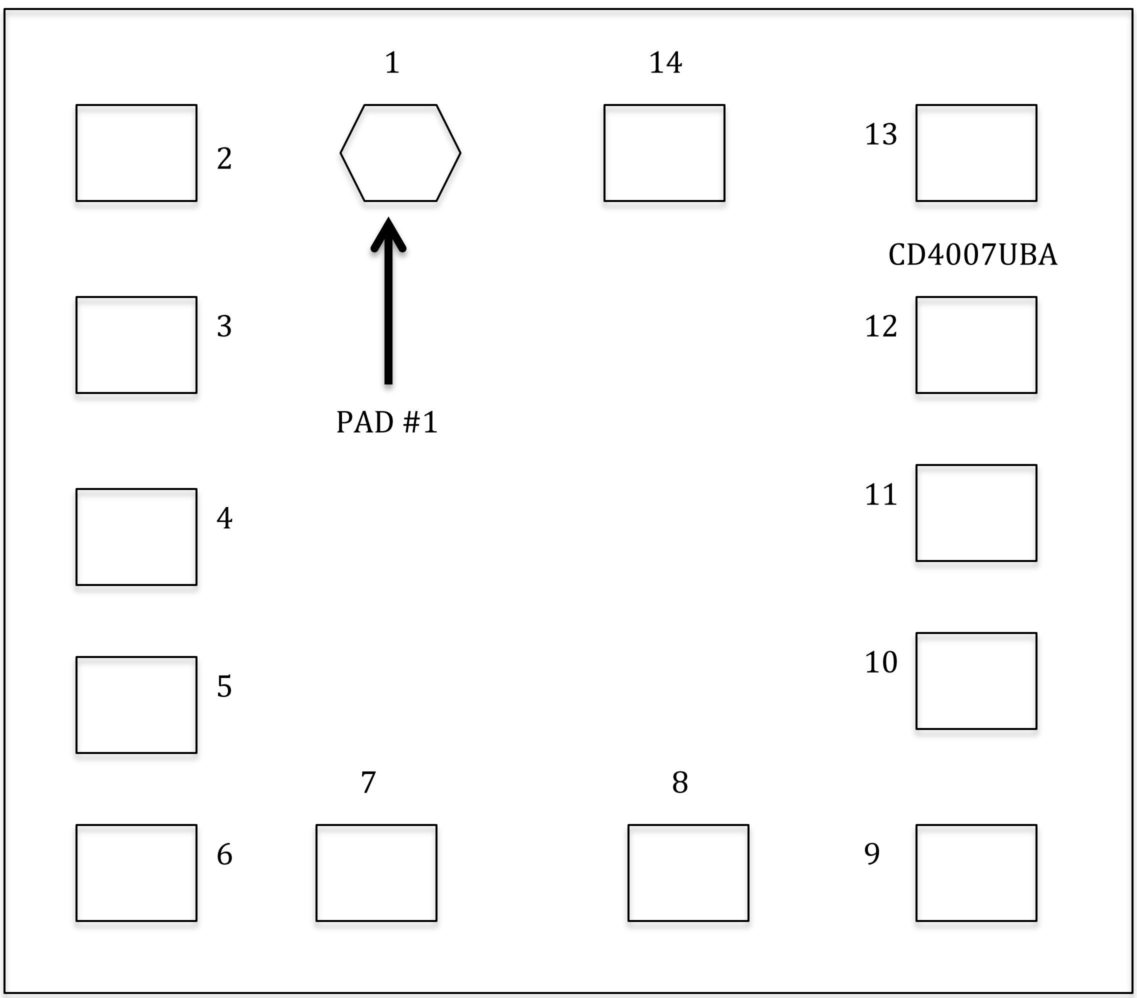


Fig 3: Microscopic view of the chip on the monitor

We can use the part of the chip where CD4007 is printed as the reference. The pin with the hexagonal shape is pin no. 1. Now moving anti-clockwise, you will see the successive pins. Therefore, the one on the left of pin no. 1, is pin no. 2 etc. The pin right above CD4007 print is pin no. 13 and the one to the left of it is pin no. 14.



The terminal diagram of the chip is as follows,

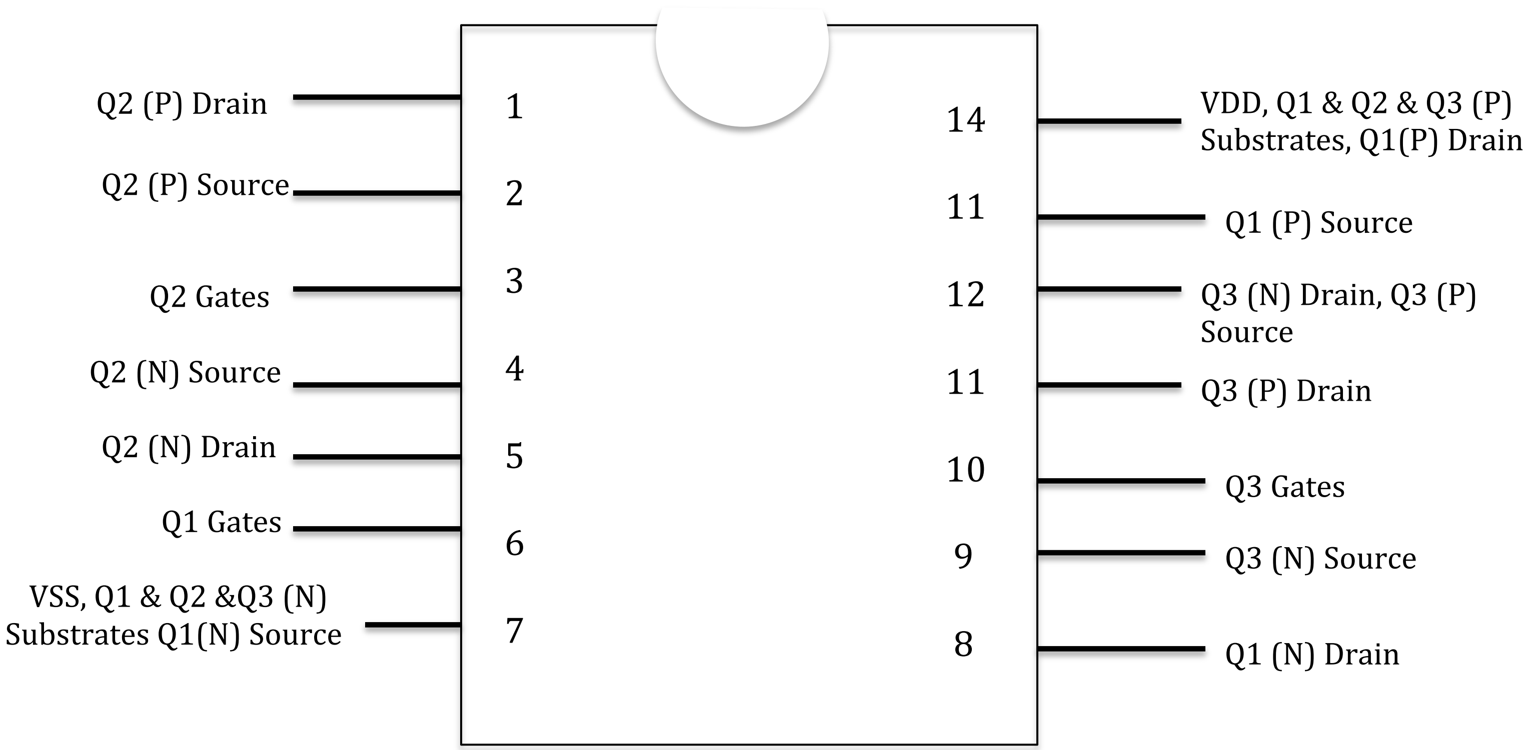


Fig. 4: Terminal diagram for CD4007UB

Therefore, looking at both the datasheet diagram and the stick diagram of the chip, we can make out the desired pins we need to place the probes at.

Chapter 4: NMOS Test

Note: After placing the probes on the appropriate pins, switch off the microscope before simulation. Also, place a black cloth over the microscope unit. This is done so that the chip is not exposed to light or any outside conditions that may alter the results. This should be done for both NMOS and PMOS test.

4.1 Procedure to test NMOS:

1. Switch on the probe station, parameter analyzer, air compressor, and the computer that has cascade's nucleus software installed in it. This computer shows the display from the microscope on the monitor. While switching the air compressor ON, along with the twisting the knob, also remember to press the 'on' button on the panel on the side of the air compressor.
2. Due to the small size of the chip, we decided to stick the chip on the bottom side of a ceramic chip. This would save base from burning during high temperatures.
3. Pull the tray of the probe station and place the chip on the chuck. Slide it back in after proper alignment of the chip.
4. Now place the probes on the chip at the correct pins looking at the monitor. For PMOS, pin 6, 7, 8 correspond to the gate, source and drain respectively.
5. Now on the Parameter Analyzer, select application mode of test, check CMOS, and the check the type of characteristic you want. First, lets start with Id-Vds characteristics. After you check this selection, the structure of MOSFET will appear. You have to enter the desired sweep for individual components.
6. For my test, I have grounded the source and provided a sweep of 0 to 5V for both the drain (Vd) and gate (Vgs), at a voltage of 1V per reading.
7. After you have entered all the values, click the 'play' button in green.
8. This should give you the desired result, along with the waveform. You can save this waveform as an image.
9. You can also save the readings by right clicking the test that appears below and save it in the format you wish.

4.2 Id-Vd test results for NMOS:

The results obtained for Id-Vds characteristics for NMOS are as follows,

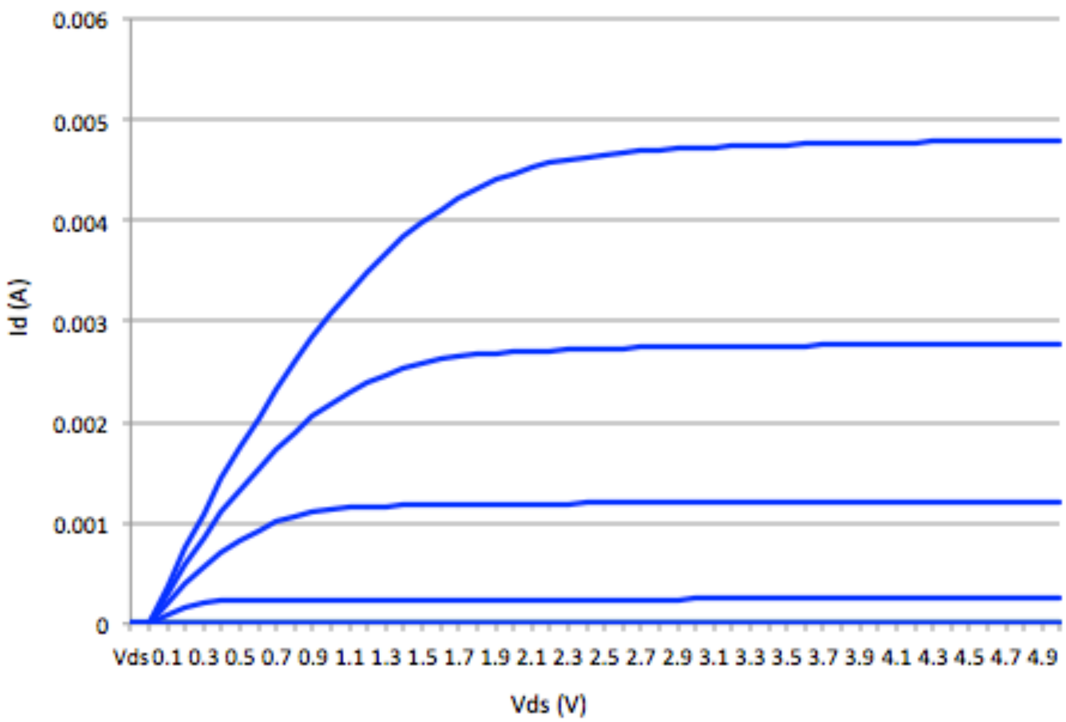


Fig. 5: Id-Vds graph for NMOS

As seen in the graph, for different values of Vgs, we obtain linear, cut-off and saturation modes over Vds.

The values obtained from the graph for Id-Vd of NMOS are as follows,

Vdrain	Vgate	Vsource	Idrain
0	0	0	2.63E-12
0.1	0	0	6.01E-12
0.2	0	0	9.69E-12
0.3	0	0	1.509E-11
0.4	0	0	1.991E-11
0.5	0	0	1.961E-11
0.6	0	0	2.199E-11
0.7	0	0	3.259E-11
0.8	0	0	8.66E-11
0.9	0	0	4.704E-11
1	0	0	1.0478E-10
1.1	0	0	5.637E-11
1.2	0	0	1.0874E-10
1.3	0	0	5.878E-11
1.4	0	0	5.742E-11
1.5	0	0	1.0958E-10
1.6	0	0	6.288E-11
1.7	0	0	6.488E-11
1.8	0	0	6.339E-11
1.9	0	0	6.405E-11
2	0	0	6.634E-11
2.1	0	0	6.716E-11
2.2	0	0	6.901E-11
2.3	0	0	7.12E-11
2.4	0	0	7.356E-11
2.5	0	0	7.581E-11
2.6	0	0	7.965E-11
2.7	0	0	7.845E-11
2.8	0	0	8.029E-11
2.9	0	0	8.448E-11
3	0	0	8.692E-11
3.1	0	0	8.809E-11
3.2	0	0	9.15E-11
3.3	0	0	9.578E-11

3.4	0	0	9.32E-11
3.5	0	0	9.88E-11
3.6	0	0	1.0264E-10
3.7	0	0	1.0356E-10
3.8	0	0	1.0644E-10
3.9	0	0	1.0999E-10
4	0	0	1.1537E-10
4.1	0	0	1.1952E-10
4.2	0	0	1.2093E-10
4.3	0	0	1.2603E-10
4.4	0	0	1.2763E-10
4.5	0	0	1.3391E-10
4.6	0	0	1.3872E-10
4.7	0	0	1.4241E-10
4.8	0	0	1.4427E-10
4.9	0	0	1.5246E-10
5	0	0	1.5902E-10
0	1	0	-4.834E-10
0.1	1	0	1.6429E-07
0.2	1	0	1.6906E-07
0.3	1	0	1.6975E-07
0.4	1	0	1.6999E-07
0.5	1	0	1.7042E-07
0.6	1	0	1.7071E-07
0.7	1	0	0.000000171
0.8	1	0	1.7113E-07
0.9	1	0	1.713E-07
1	1	0	1.7148E-07
1.1	1	0	1.7159E-07
1.2	1	0	1.7177E-07
1.3	1	0	1.7192E-07
1.4	1	0	1.7207E-07
1.5	1	0	1.7211E-07
1.6	1	0	1.7241E-07
1.7	1	0	1.7241E-07
1.8	1	0	1.724E-07
1.9	1	0	1.7268E-07
2	1	0	1.7278E-07
2.1	1	0	1.7281E-07
2.2	1	0	1.7303E-07

2.3	1	0	1.7303E-07
2.4	1	0	1.7317E-07
2.5	1	0	1.732E-07
2.6	1	0	1.7335E-07
2.7	1	0	1.7344E-07
2.8	1	0	1.7364E-07
2.9	1	0	1.7373E-07
3	1	0	1.7379E-07
3.1	1	0	1.7392E-07
3.2	1	0	0.000000174
3.3	1	0	1.7404E-07
3.4	1	0	1.7414E-07
3.5	1	0	1.7429E-07
3.6	1	0	1.7423E-07
3.7	1	0	1.7443E-07
3.8	1	0	1.7445E-07
3.9	1	0	1.7458E-07
4	1	0	1.7516E-07
4.1	1	0	1.7533E-07
4.2	1	0	1.7545E-07
4.3	1	0	1.7539E-07
4.4	1	0	1.7544E-07
4.5	1	0	1.7563E-07
4.6	1	0	1.7559E-07
4.7	1	0	1.7574E-07
4.8	1	0	1.7588E-07
4.9	1	0	1.7581E-07
5	1	0	1.7591E-07
0	2	0	-9.5837E-08
0.1	2	0	0.000094448
0.2	2	0	0.00016097
0.3	2	0	0.00020209
0.4	2	0	0.00022289
0.5	2	0	0.00023145
0.6	2	0	0.00023483
0.7	2	0	0.00023647
0.8	2	0	0.00023745
0.9	2	0	0.0002382
1	2	0	0.00023878
1.1	2	0	0.00023921

1.2	2	0	0.00023966
1.3	2	0	0.00023999
1.4	2	0	0.00024032
1.5	2	0	0.00024059
1.6	2	0	0.00024089
1.7	2	0	0.0002411
1.8	2	0	0.00024132
1.9	2	0	0.00024154
2	2	0	0.00024176
2.1	2	0	0.00024197
2.2	2	0	0.00024214
2.3	2	0	0.00024231
2.4	2	0	0.00024251
2.5	2	0	0.00024271
2.6	2	0	0.00024284
2.7	2	0	0.00024298
2.8	2	0	0.00024317
2.9	2	0	0.00024331
3	2	0	0.00024348
3.1	2	0	0.0002436
3.2	2	0	0.00024371
3.3	2	0	0.00024385
3.4	2	0	0.00024402
3.5	2	0	0.00024414
3.6	2	0	0.00024431
3.7	2	0	0.00024442
3.8	2	0	0.00024453
3.9	2	0	0.00024465
4	2	0	0.0002448
4.1	2	0	0.00024492
4.2	2	0	0.00024507
4.3	2	0	0.00024519
4.4	2	0	0.00024531
4.5	2	0	0.00024542
4.6	2	0	0.00024549
4.7	2	0	0.00024558
4.8	2	0	0.0002457
4.9	2	0	0.00024581
5	2	0	0.00024592
0	3	0	-1.16744E-07

0.1	3	0	0.0002115
0.2	3	0	0.00040022
0.3	3	0	0.00056628
0.4	3	0	0.00070927
0.5	3	0	0.00082975
0.6	3	0	0.0009284
0.7	3	0	0.00100583
0.8	3	0	0.00106344
0.9	3	0	0.00110408
1	3	0	0.00113101
1.1	3	0	0.00114814
1.2	3	0	0.0011593
1.3	3	0	0.0011666
1.4	3	0	0.0011721
1.5	3	0	0.0011758
1.6	3	0	0.0011792
1.7	3	0	0.001182
1.8	3	0	0.0011841
1.9	3	0	0.0011862
2	3	0	0.0011878
2.1	3	0	0.0011893
2.2	3	0	0.0011911
2.3	3	0	0.0011922
2.4	3	0	0.0011937
2.5	3	0	0.0011949
2.6	3	0	0.0011959
2.7	3	0	0.0011968
2.8	3	0	0.0011979
2.9	3	0	0.0011987
3	3	0	0.0011998
3.1	3	0	0.0012005
3.2	3	0	0.0012014
3.3	3	0	0.0012022
3.4	3	0	0.0012029
3.5	3	0	0.0012039
3.6	3	0	0.0012045
3.7	3	0	0.0012051
3.8	3	0	0.001206
3.9	3	0	0.0012068
4	3	0	0.0012075

4.1	3	0	0.001208
4.2	3	0	0.0012086
4.3	3	0	0.0012094
4.4	3	0	0.0012098
4.5	3	0	0.0012105
4.6	3	0	0.0012109
4.7	3	0	0.0012116
4.8	3	0	0.001212
4.9	3	0	0.0012127
5	3	0	0.0012133
0	4	0	-6.3613E-08
0.1	4	0	0.00030483
0.2	4	0	0.00059081
0.3	4	0	0.00085722
0.4	4	0	0.0011052
0.5	4	0	0.0013335
0.6	4	0	0.0015432
0.7	4	0	0.0017333
0.8	4	0	0.0019035
0.9	4	0	0.002055
1	4	0	0.0021871
1.1	4	0	0.0023006
1.2	4	0	0.0023963
1.3	4	0	0.0024742
1.4	4	0	0.0025367
1.5	4	0	0.0025847
1.6	4	0	0.0026212
1.7	4	0	0.0026484
1.8	4	0	0.0026685
1.9	4	0	0.0026836
2	4	0	0.002695
2.1	4	0	0.0027044
2.2	4	0	0.0027119
2.3	4	0	0.002718
2.4	4	0	0.0027234
2.5	4	0	0.0027282
2.6	4	0	0.0027326
2.7	4	0	0.002736
2.8	4	0	0.0027392
2.9	4	0	0.0027425

3	4	0	0.0027453
3.1	4	0	0.0027479
3.2	4	0	0.0027503
3.3	4	0	0.0027527
3.4	4	0	0.0027549
3.5	4	0	0.0027568
3.6	4	0	0.002759
3.7	4	0	0.0027608
3.8	4	0	0.0027624
3.9	4	0	0.0027642
4	4	0	0.0027659
4.1	4	0	0.0027676
4.2	4	0	0.002769
4.3	4	0	0.0027703
4.4	4	0	0.0027716
4.5	4	0	0.0027732
4.6	4	0	0.0027744
4.7	4	0	0.0027756
4.8	4	0	0.0027768
4.9	4	0	0.0027778
5	4	0	0.0027793
0	5	0	-6.9271E-08
0.1	5	0	0.00038192
0.2	5	0	0.00074743
0.3	5	0	0.00109675
0.4	5	0	0.0014308
0.5	5	0	0.0017465
0.6	5	0	0.0020468
0.7	5	0	0.0023305
0.8	5	0	0.0025958
0.9	5	0	0.0028457
1	5	0	0.0030777
1.1	5	0	0.0032922
1.2	5	0	0.0034897
1.3	5	0	0.00367
1.4	5	0	0.003833
1.5	5	0	0.003979
1.6	5	0	0.0041077
1.7	5	0	0.0042206
1.8	5	0	0.0043176

1.9	5	0	0.0043997
2	5	0	0.0044674
2.1	5	0	0.0045235
2.2	5	0	0.0045688
2.3	5	0	0.0046045
2.4	5	0	0.004633
2.5	5	0	0.004656
2.6	5	0	0.0046742
2.7	5	0	0.0046893
2.8	5	0	0.0047018
2.9	5	0	0.0047123
3	5	0	0.0047212
3.1	5	0	0.0047291
3.2	5	0	0.0047359
3.3	5	0	0.0047421
3.4	5	0	0.0047474
3.5	5	0	0.0047526
3.6	5	0	0.004757
3.7	5	0	0.0047611
3.8	5	0	0.0047648
3.9	5	0	0.0047684
4	5	0	0.0047716
4.1	5	0	0.0047745
4.2	5	0	0.0047772
4.3	5	0	0.00478
4.4	5	0	0.0047826
4.5	5	0	0.0047847
4.6	5	0	0.004787
4.7	5	0	0.0047892
4.8	5	0	0.0047915
4.9	5	0	0.0047932
5	5	0	0.0047946

4.3 Id- Vgs test for NMOS:

Along with Id-Vds, we will also analyze the Id-Vgs characteristics. The procedure to select this mode is similar to Id-Vds selection. Select Application test, check CMOS, and then check Id-Vgs.

We will perform Id-Vgs for Vd= 5V. Vgs will range from 0 to 5V and source is given 0V.

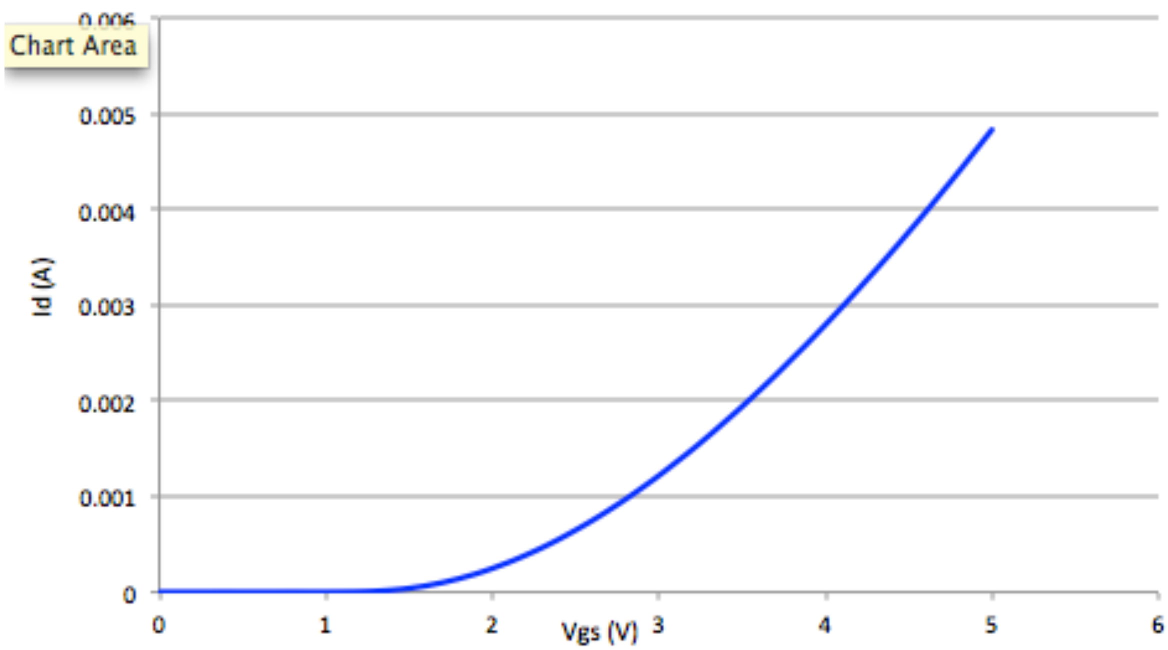


Fig. 6: Id-Vgs characteristics for NMOS

The values obtained from the graph are as follows:

Vgate	Vdrain	Vsource	Idrain
0	5	0	0.0000005
0.1	5	0	0.0000005
0.2	5	0	0.0000005
0.3	5	0	0.0000005
0.4	5	0	0.000001
0.5	5	0	0.0000005
0.6	5	0	0.0000005
0.7	5	0	0.0000005
0.8	5	0	0.000001
0.9	5	0	0.0000005
1	5	0	0.0000005
1.1	5	0	0.0000015
1.2	5	0	0.0000035
1.3	5	0	0.0000095
1.4	5	0	0.0000205
1.5	5	0	0.0000385
1.6	5	0	0.0000645
1.7	5	0	0.0000985
1.8	5	0	0.00014
1.9	5	0	0.0001895
2	5	0	0.000247
2.1	5	0	0.000312
2.2	5	0	0.000385
2.3	5	0	0.0004645
2.4	5	0	0.000552
2.5	5	0	0.000647
2.6	5	0	0.0007475
2.7	5	0	0.0008555
2.8	5	0	0.0009695
2.9	5	0	0.0010905
3	5	0	0.0012165
3.1	5	0	0.001351
3.2	5	0	0.001488
3.3	5	0	0.0016335

3.4	5	0	0.0017845
3.5	5	0	0.0019385
3.6	5	0	0.0020995
3.7	5	0	0.0022645
3.8	5	0	0.0024375
3.9	5	0	0.0026115
4	5	0	0.002793
4.1	5	0	0.002978
4.2	5	0	0.0031675
4.3	5	0	0.003361
4.4	5	0	0.0035585
4.5	5	0	0.0037615
4.6	5	0	0.003967
4.7	5	0	0.004177
4.8	5	0	0.0043905
4.9	5	0	0.00461
5	5	0	0.0048305

The above readings have been obtained by keep the drain voltage as constant 5V. The gate voltage is varied from 0 to 5V. The source is grounded.

The Id-Vgs in log scale can be obtained by getting into the settings menu from the graph screen. There is an option to change the scale for individual axis. Change the Y-axis from linear to log scale. This way we obtain the Id-Vds characteristics in log scale.

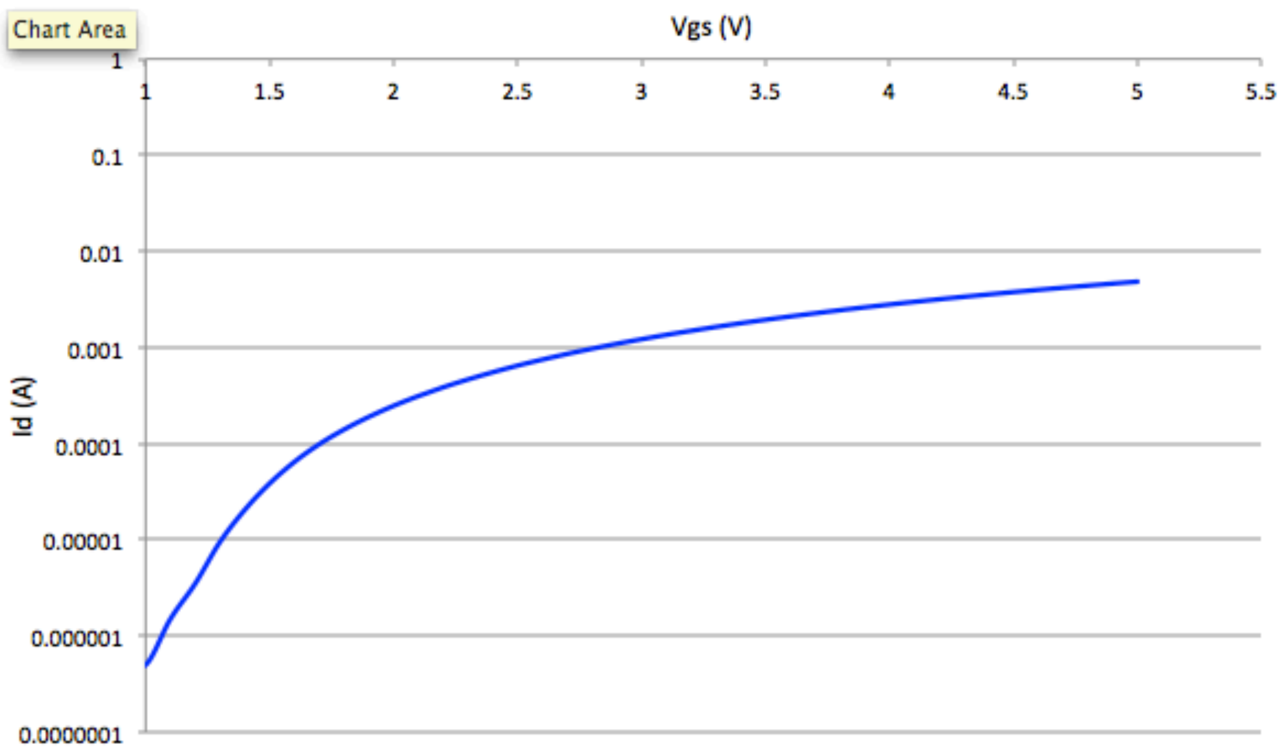


Fig. 7: Id-Vgs characteristics in log scale.

Chapter 5: PMOS Test

5.1 Procedure to test PMOS:

1. Switch on the probe station, parameter analyzer, air compressor, and the computer that has cascade's nucleus software installed in it. This computer shows the display from the microscope on the monitor. While switching the air compressor ON, along with the twisting the knob, also remember to press the 'on' button on the panel on the side of the air compressor.
2. Due to the small size of the chip, we decided to stick the chip on the bottom side of a ceramic chip. This would save base from burning during high temperatures.
3. Pull the tray of the probe station and place the chip on the chuck. Slide it back in after proper alignment of the chip.
4. Now place the probes on the chip at the correct pins looking at the monitor. For PMOS, pin 6, 7, 8 correspond to the gate source and drain respectively.
5. Now on the Parameter Analyzer, select application mode of test, check CMOS, and the check the type of characteristic you want. First, lets start with Id-Vds characteristics. After you check this selection, the structure of MOSFET will appear. You have to enter the desired sweep for individual components.
6. For my test, I have grounded the source and provided a sweep of 0 to 5V for both the drain (Vd) and gate (Vgs), at a voltage of 1V per reading.
7. After you have entered all the values, click the 'play' button in green.
8. This should give you the desired result, along with the waveform. You can save this waveform as an image.
9. You can also save the readings by right clicking the test that appears below and save it in the format you wish.

5.2 Id-Vd results for PMOS:

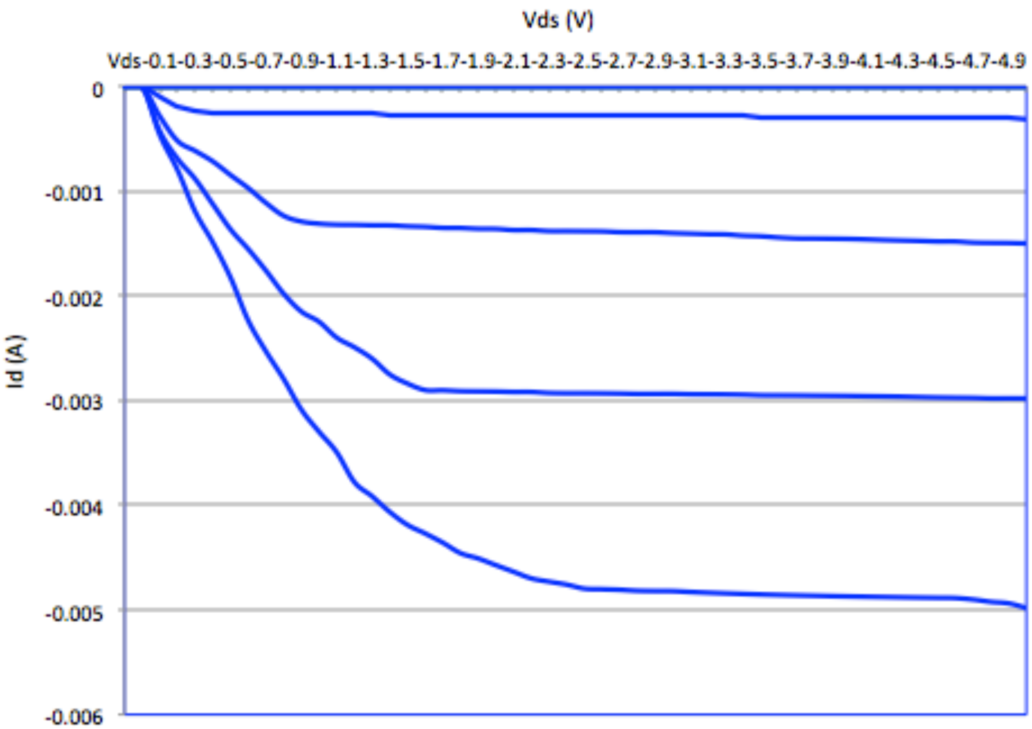


Fig 8: Id-Vd graph for PMOS

As seen in the graph, for different negative values of Vgs, we obtain linear, cut-off and saturation modes over different values of Vds.

The readings obtained from the graph For Id-Vd of PMOS are as follows,

Vdrain	Vgate	Vsource	Idrain
0	0	0	-5.37E-12
-0.1	0	0	-6.31E-12
-0.2	0	0	-9.27E-12
-0.3	0	0	-1.689E-11
-0.4	0	0	-1.791E-11
-0.5	0	0	-1.8996E-11
-0.6	0	0	-2.468E-11
-0.7	0	0	-3.225E-11
-0.8	0	0	-6.908E-11
-0.9	0	0	-8.704E-11
-1	0	0	-1.1238E-11
-1.1	0	0	-6.237E-11
-1.2	0	0	-6.237E-11
-1.3	0	0	-6.478E-11
-1.4	0	0	-7.02342E-11
-1.5	0	0	-1.0958E-11
-1.6	0	0	-6.288E-11
-1.7	0	0	-7.988E-11
-1.8	0	0	-8.039E-11
-1.9	0	0	-8.205E-11
-2	0	0	-8.334E-11
-2.1	0	0	-8.579E-11
-2.2	0	0	-8.801E-11
-2.3	0	0	-8.12E-11
-2.4	0	0	-8.356E-11
-2.5	0	0	-8.581E-11
-2.6	0	0	-8.965E-11
-2.7	0	0	-8.845E-11
-2.8	0	0	-9.029E-11
-2.9	0	0	-9.448E-11
-3	0	0	-9.692E-11
-3.1	0	0	-9.809E-11
-3.2	0	0	-1.015E-11

-3.3	0	0	-1.0578E-10
-3.4	0	0	-1.082E-10
-3.5	0	0	-1.092E-10
-3.6	0	0	-1.09644E-10
-3.7	0	0	-1.2356E-10
-3.8	0	0	-1.2644E-10
-3.9	0	0	-1.1399E-10
-4	0	0	-1.1537E-10
-4.1	0	0	-1.2352E-10
-4.2	0	0	-1.3093E-10
-4.3	0	0	-1.3203E-10
-4.4	0	0	-1.3963E-10
-4.5	0	0	-1.4591E-10
-4.6	0	0	-1.5072E-10
-4.7	0	0	-1.6041E-10
-4.8	0	0	-1.6327E-10
-4.9	0	0	-1.6446E-10
-5	0	0	-1.6902E-10
0	-1	0	4.834E-10
-0.1	-1	0	-1.75334E-07
-0.2	-1	0	-1.77651E-07
-0.3	-1	0	-1.89007E-07
-0.4	-1	0	-1.85434E-07
-0.5	-1	0	-1.8999E-07
-0.6	-1	0	-1.95223E-07
-0.7	-1	0	-2.05223E-07
-0.8	-1	0	-2.0613E-07
-0.9	-1	0	-2.0713E-07
-1	-1	0	-2.1148E-07
-1.1	-1	0	-2.1159E-07
-1.2	-1	0	-2.1177E-07
-1.3	-1	0	-2.1192E-07
-1.4	-1	0	-2.1207E-07
-1.5	-1	0	-2.1211E-07
-1.6	-1	0	-2.1241E-07
-1.7	-1	0	-2.1241E-07
-1.8	-1	0	-2.124E-07
-1.9	-1	0	-2.1268E-07
-2	-1	0	-2.1278E-07
-2.1	-1	0	-2.1281E-07

-2.2	-1	0	-2.1303E-07
-2.3	-1	0	-2.1303E-07
-2.4	-1	0	-2.1309E-07
-2.5	-1	0	-2.132E-07
-2.6	-1	0	-2.1335E-07
-2.7	-1	0	-2.1344E-07
-2.8	-1	0	-2.1364E-07
-2.9	-1	0	-2.1373E-07
-3	-1	0	-2.1379E-07
-3.1	-1	0	-2.1392E-07
-3.2	-1	0	-2.1392E-07
-3.3	-1	0	-2.1404E-07
-3.4	-1	0	-2.1414E-07
-3.5	-1	0	-2.1429E-07
-3.6	-1	0	-2.1423E-07
-3.7	-1	0	-2.1443E-07
-3.8	-1	0	-2.1445E-07
-3.9	-1	0	-2.1458E-07
-4	-1	0	-2.1516E-07
-4.1	-1	0	-2.1533E-07
-4.2	-1	0	-2.1545E-07
-4.3	-1	0	-2.1539E-07
-4.4	-1	0	-2.1544E-07
-4.5	-1	0	-2.1563E-07
-4.6	-1	0	-2.1559E-07
-4.7	-1	0	-2.1574E-07
-4.8	-1	0	-2.1588E-07
-4.9	-1	0	-2.1581E-07
-5	-1	0	-2.1591E-07
0	-2	0	9.5837E-08
-0.1	-2	0	-0.000094448
-0.2	-2	0	-0.00018097
-0.3	-2	0	-0.000232209
-0.4	-2	0	-0.000243289
-0.5	-2	0	-0.00025194
-0.6	-2	0	-0.000252345
-0.7	-2	0	-0.000253013
-0.8	-2	0	-0.000254374
-0.9	-2	0	-0.000255679
-1	-2	0	-0.000256978

-1.1	-2	0	-0.00025701
-1.2	-2	0	-0.000258127
-1.3	-2	0	-0.000259933
-1.4	-2	0	-0.00027903
-1.5	-2	0	-0.00027059
-1.6	-2	0	-0.00027089
-1.7	-2	0	-0.0002711
-1.8	-2	0	-0.000272132
-1.9	-2	0	-0.000273154
-2	-2	0	-0.000273976
-2.1	-2	0	-0.000274197
-2.2	-2	0	-0.000275214
-2.3	-2	0	-0.000277231
-2.4	-2	0	-0.000278251
-2.5	-2	0	-0.000281271
-2.6	-2	0	-0.000282284
-2.7	-2	0	-0.00028398
-2.8	-2	0	-0.000284317
-2.9	-2	0	-0.000284431
-3	-2	0	-0.000284846
-3.1	-2	0	-0.00028496
-3.2	-2	0	-0.0002851
-3.3	-2	0	-0.0002853
-3.4	-2	0	-0.0002854
-3.5	-2	0	-0.0002855
-3.6	-2	0	-0.0002856
-3.7	-2	0	-0.0002857
-3.8	-2	0	-0.0002859
-3.9	-2	0	-0.000291
-4	-2	0	-0.00029234
-4.1	-2	0	-0.000293
-4.2	-2	0	-0.0002939
-4.3	-2	0	-0.00029421
-4.4	-2	0	-0.00029592
-4.5	-2	0	-0.00029603
-4.6	-2	0	-0.000297032
-4.7	-2	0	-0.00029883
-4.8	-2	0	-0.000299399
-4.9	-2	0	-0.00030001
-5	-2	0	-0.000312385

0	-3	0	1.16744E-07
-0.1	-3	0	-0.00028465
-0.2	-3	0	-0.00051934
-0.3	-3	0	-0.000614963
-0.4	-3	0	-0.000715799
-0.5	-3	0	-0.00084569
-0.6	-3	0	-0.000970088
-0.7	-3	0	-0.001111861
-0.8	-3	0	-0.001234563
-0.9	-3	0	-0.00128943
-1	-3	0	-0.0013101
-1.1	-3	0	-0.001319383
-1.2	-3	0	-0.001321159
-1.3	-3	0	-0.001324829
-1.4	-3	0	-0.001325952
-1.5	-3	0	-0.001334729
-1.6	-3	0	-0.001340122
-1.7	-3	0	-0.00135
-1.8	-3	0	-0.001351284
-1.9	-3	0	-0.00135862
-2	-3	0	-0.001360138
-2.1	-3	0	-0.001370993
-2.2	-3	0	-0.001371246
-2.3	-3	0	-0.001380754
-2.4	-3	0	-0.001381294
-2.5	-3	0	-0.00138249
-2.6	-3	0	-0.001383959
-2.7	-3	0	-0.00139068
-2.8	-3	0	-0.001391979
-2.9	-3	0	-0.001392399
-3	-3	0	-0.0013998
-3.1	-3	0	-0.001405005
-3.2	-3	0	-0.001409901
-3.3	-3	0	-0.0014122
-3.4	-3	0	-0.00142469
-3.5	-3	0	-0.001430464
-3.6	-3	0	-0.0014424
-3.7	-3	0	-0.0014509
-3.8	-3	0	-0.001452
-3.9	-3	0	-0.00145349

-4	-3	0	-0.00145579
-4.1	-3	0	-0.00146019
-4.2	-3	0	-0.001466136
-4.3	-3	0	-0.001470754
-4.4	-3	0	-0.00147468
-4.5	-3	0	-0.001479744
-4.6	-3	0	-0.00148054
-4.7	-3	0	-0.001490753
-4.8	-3	0	-0.00149358
-4.9	-3	0	-0.001494678
-5	-3	0	-0.001498654
0	-4	0	6.3613E-08
-0.1	-4	0	-0.000428048
-0.2	-4	0	-0.000689608
-0.3	-4	0	-0.000883832
-0.4	-4	0	-0.001125484
-0.5	-4	0	-0.001365314
-0.6	-4	0	-0.00155332
-0.7	-4	0	-0.001758833
-0.8	-4	0	-0.00197935
-0.9	-4	0	-0.0021495
-1	-4	0	-0.0022468
-1.1	-4	0	-0.002398906
-1.2	-4	0	-0.002490776
-1.3	-4	0	-0.002599542
-1.4	-4	0	-0.002750367
-1.5	-4	0	-0.002837647
-1.6	-4	0	-0.002900212
-1.7	-4	0	-0.002902338
-1.8	-4	0	-0.002910233
-1.9	-4	0	-0.002912344
-2	-4	0	-0.002913844
-2.1	-4	0	-0.002917833
-2.2	-4	0	-0.002918364
-2.3	-4	0	-0.002927364
-2.4	-4	0	-0.00292999
-2.5	-4	0	-0.002930134
-2.6	-4	0	-0.002931039
-2.7	-4	0	-0.00293294
-2.8	-4	0	-0.002935943

-2.9	-4	0	-0.00293598
-3	-4	0	-0.002936024
-3.1	-4	0	-0.002939284
-3.2	-4	0	-0.002940243
-3.3	-4	0	-0.002941294
-3.4	-4	0	-0.002943828
-3.5	-4	0	-0.0029492
-3.6	-4	0	-0.002950193
-3.7	-4	0	-0.002951029
-3.8	-4	0	-0.002952849
-3.9	-4	0	-0.00295422
-4	-4	0	-0.002955838
-4.1	-4	0	-0.002958249
-4.2	-4	0	-0.002960283
-4.3	-4	0	-0.002962939
-4.4	-4	0	-0.002966832
-4.5	-4	0	-0.002970384
-4.6	-4	0	-0.002972637
-4.7	-4	0	-0.002974638
-4.8	-4	0	-0.00297897
-4.9	-4	0	-0.002979054
-5	-4	0	-0.0029797
0	-5	0	6.9271E-08
-0.1	-5	0	-0.00046192
-0.2	-5	0	-0.00079743
-0.3	-5	0	-0.00119675
-0.4	-5	0	-0.0014908
-0.5	-5	0	-0.0018265
-0.6	-5	0	-0.0022368
-0.7	-5	0	-0.0025305
-0.8	-5	0	-0.00279358
-0.9	-5	0	-0.00308657
-1	-5	0	-0.003297788
-1.1	-5	0	-0.003493922
-1.2	-5	0	-0.003779297
-1.3	-5	0	-0.003914686
-1.4	-5	0	-0.004064474
-1.5	-5	0	-0.004188
-1.6	-5	0	-0.004269946
-1.7	-5	0	-0.004357928

-1.8	-5	0	-0.004457909
-1.9	-5	0	-0.004508644
-2	-5	0	-0.004572924
-2.1	-5	0	-0.004635764
-2.2	-5	0	-0.00469907
-2.3	-5	0	-0.004730203
-2.4	-5	0	-0.00475833
-2.5	-5	0	-0.00479727
-2.6	-5	0	-0.004802739
-2.7	-5	0	-0.00480783
-2.8	-5	0	-0.004817273
-2.9	-5	0	-0.004820122
-3	-5	0	-0.0048212
-3.1	-5	0	-0.0048291
-3.2	-5	0	-0.0048359
-3.3	-5	0	-0.0048421
-3.4	-5	0	-0.0048474
-3.5	-5	0	-0.0048526
-3.6	-5	0	-0.004857
-3.7	-5	0	-0.0048611
-3.8	-5	0	-0.0048648
-3.9	-5	0	-0.0048684
-4	-5	0	-0.0048716
-4.1	-5	0	-0.0048745
-4.2	-5	0	-0.0048772
-4.3	-5	0	-0.00488
-4.4	-5	0	-0.0048826
-4.5	-5	0	-0.0048847
-4.6	-5	0	-0.004887
-4.7	-5	0	-0.00490122
-4.8	-5	0	-0.004923475
-4.9	-5	0	-0.004937773
-5	-5	0	-0.004981724

5.3 Id-Vgs results for PMOS:

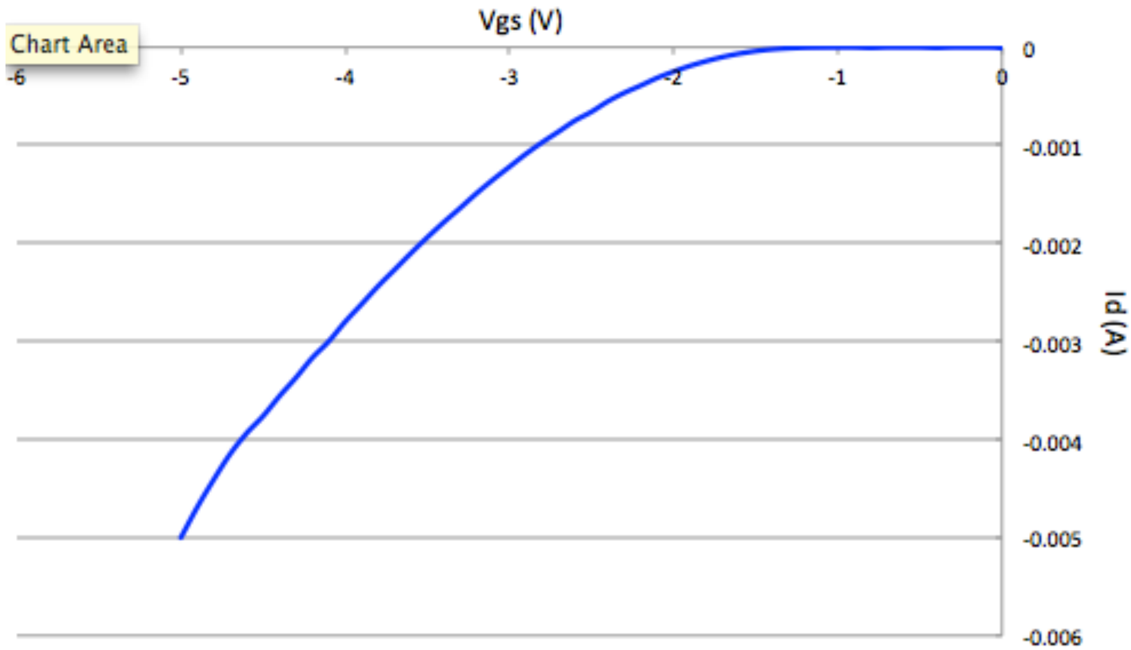


Fig 9: Id-Vgs graph for PMOS

Along with Id-Vds, we will also analyze the Id-Vgs characteristics. The procedure to select this mode is similar to Id-Vds selection. Select Application test, check CMOS, and then check Id-Vgs.

We will perform Id-Vgs for Vd= -5V. Vgs will range from 0 to -5V and source is given 0V.

The values obtained from the graph for Id-Vgs from PMOS are as follows:

Vgate	Vdrain	Vsource	Idrain
0	-5	0	-0.0000005
-0.1	-5	0	-0.0000005
-0.2	-5	0	-0.0000005
-0.3	-5	0	-0.0000005
-0.4	-5	0	-0.000005
-0.5	-5	0	-0.0000005
-0.6	-5	0	-0.0000005
-0.7	-5	0	-0.0000005
-0.8	-5	0	-0.000005
-0.9	-5	0	-0.0000005
-1	-5	0	-0.0000005
-1.1	-5	0	-1.50267E-06
-1.2	-5	0	-3.50136E-06
-1.3	-5	0	-9.50135E-06
-1.4	-5	0	-2.05103E-05
-1.5	-5	0	-3.85064E-05
-1.6	-5	0	-6.45104E-05
-1.7	-5	0	-9.85085E-05
-1.8	-5	0	-1.41E-04
-1.9	-5	0	-0.00019
-2	-5	0	-0.000248139
-2.1	-5	0	-0.000312566
-2.2	-5	0	-0.000390364
-2.3	-5	0	-0.000464604
-2.4	-5	0	-0.000552017
-2.5	-5	0	-0.00065808
-2.6	-5	0	-0.000747696
-2.7	-5	0	-0.000860157
-2.8	-5	0	-0.000970001
-2.9	-5	0	-0.001089
-3	-5	0	-0.001219865
-3.1	-5	0	-0.001351012
-3.2	-5	0	-0.001490356
-3.3	-5	0	-0.001640124

-3.4	-5	0	-0.001785946
-3.5	-5	0	-0.001939375
-3.6	-5	0	-0.002101257
-3.7	-5	0	-0.002270184
-3.8	-5	0	-0.0024375
-3.9	-5	0	-0.002620385
-4	-5	0	-0.002800043
-4.1	-5	0	-0.00300002
-4.2	-5	0	-0.0031675
-4.3	-5	0	-0.003370347
-4.4	-5	0	-0.0035585
-4.5	-5	0	-0.003762137
-4.6	-5	0	-0.003936777
-4.7	-5	0	-0.004147939
-4.8	-5	0	-0.004408491
-4.9	-5	0	-0.004689234
-5	-5	0	-0.005000283

The Id-Vgs in log scale was obtained by taking positive values instead of the negative values obtained.

The resultant graph is as follows,

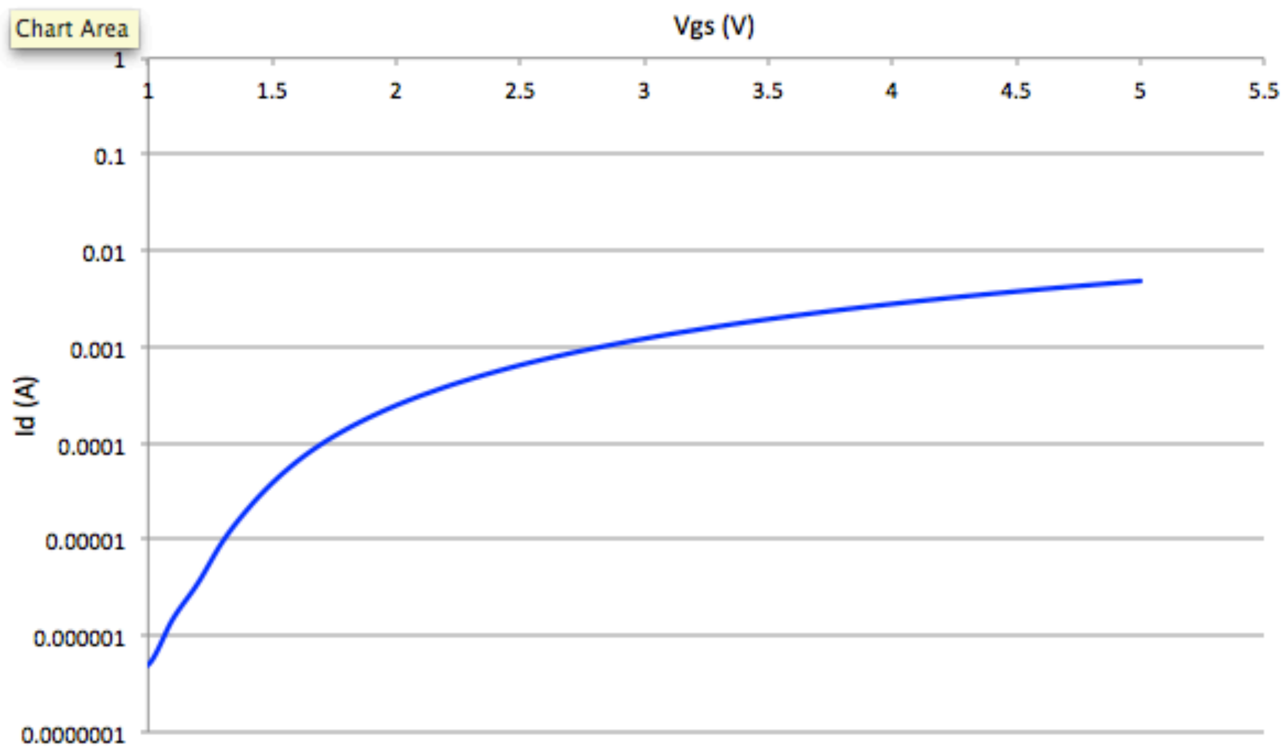


Fig 10: Id-Vgs Log scale for PMOS

Chapter 6: Calculation of MOSFET parameters:

The saturation equation for current is given by,

$i= k/2\ (V-Vt)\ (1+\lambda V)$

Therefore, $k/2(V-Vt)^2 = i/(1 +\lambda V)$

$\sqrt{k/2}\ (V-Vt) = \sqrt{(i/1 +\lambda V)}$

To plot the I-V graph for this equation, we take,
$x = V$, $y = \sqrt{(i/1 +\lambda V)}$

NMOS calculation:

λ_n Calculation:

First, we will need to calculate λ, the channel length modulation factor.

For this purpose, we will have to consider one Id-Vds graph for a single value of Vgs,
Considering Vgs= 4V,

Id vs Vds for Vgs=4V

$\lambda n = 1/ (r_0 I_D - V_{SD})$, where $1/r_0$ is the slope of the graph,

In order to consider the slope, lets consider values of Id Vds=4V and Vds=5V,

$$\text{Therefore, } i/r_0 = \frac{\text{Id(for Vds=5)-Id(for Vds=4)}}{5-4}$$

$1/r_0 = (0.0027793\text{-}0.0027659)/1$

Therefore, $r_0 = 74{,}626.865$

Since, $\lambda n = 1/ (r_0 I_D - V_{DS})$,

For Vds= 4V,

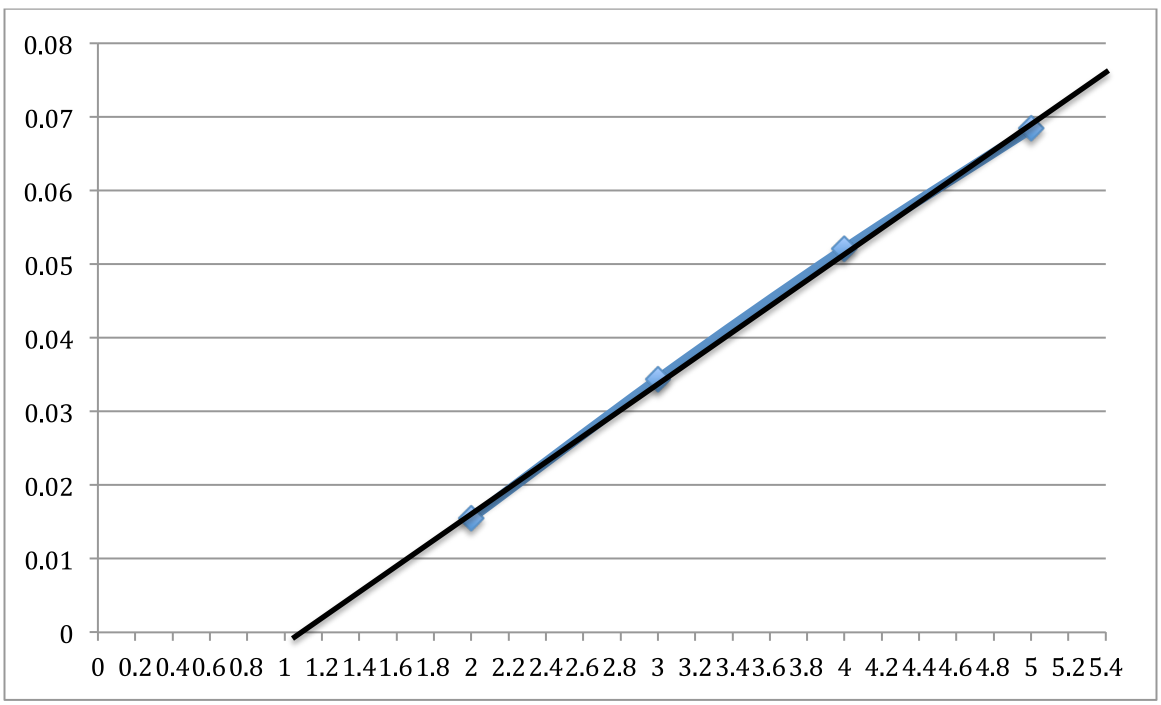
$\lambda n = 1/(206.4104-4)$

Hence, $\underline{\lambda n = 0.00494 V^{-1}}$

In order to obtain Vt for NMOS, we will need the current values at which Vds=Vgs,

i (Amps)	x = V (volts)	y= √(i/1+λV)
0.00000017148	1	0.00041251
0.00024176	2	0.015473
0.0011998	3	0.034386
0.0027659	4	0.052083
0.0047946	5	0.06841

Plotting the values for x and y, we get,



Now make the best-fit line for the graph and wherever it intersects the x-axis is the threshold voltage. Here Vt= 0.98V.

Calculating Kn:

Kn = $2s^2$, where s is the slope of the best-fit line.

From the graph, s= 0.02-0.01/2.2-1.6 = 0.01666

Kn = $2(0.01666)^2 = 5.5 \times 10^{-4}$ A/V^2

PMOS Calculation:

λ_p Calculation:

First, we will need to calculate λ, the channel length modulation factor.

For this purpose, we will have to consider one Id-Vds graph for a single value of Vgs,
Considering Vgs= -4V,

$\lambda p = 1/ (r_0 I_D - V_{DS})$, where $1/r_0$ is the slope of the graph,

In order to consider the slope, lets consider values of Id Vds=-4V and Vds=-5V,

$$\text{Therefore, } 1/r_0 = \frac{\text{Id(for Vds=-5)-Id(for Vds=-4)}}{-5-(-4)}$$

$1/r_0$ = -0.0029797- (-0.002955838)/1

r_0= 41,907.6385

Since, $\lambda p = 1/ (r_0 I_D - V_{SD})$,

For Vds= -4V,

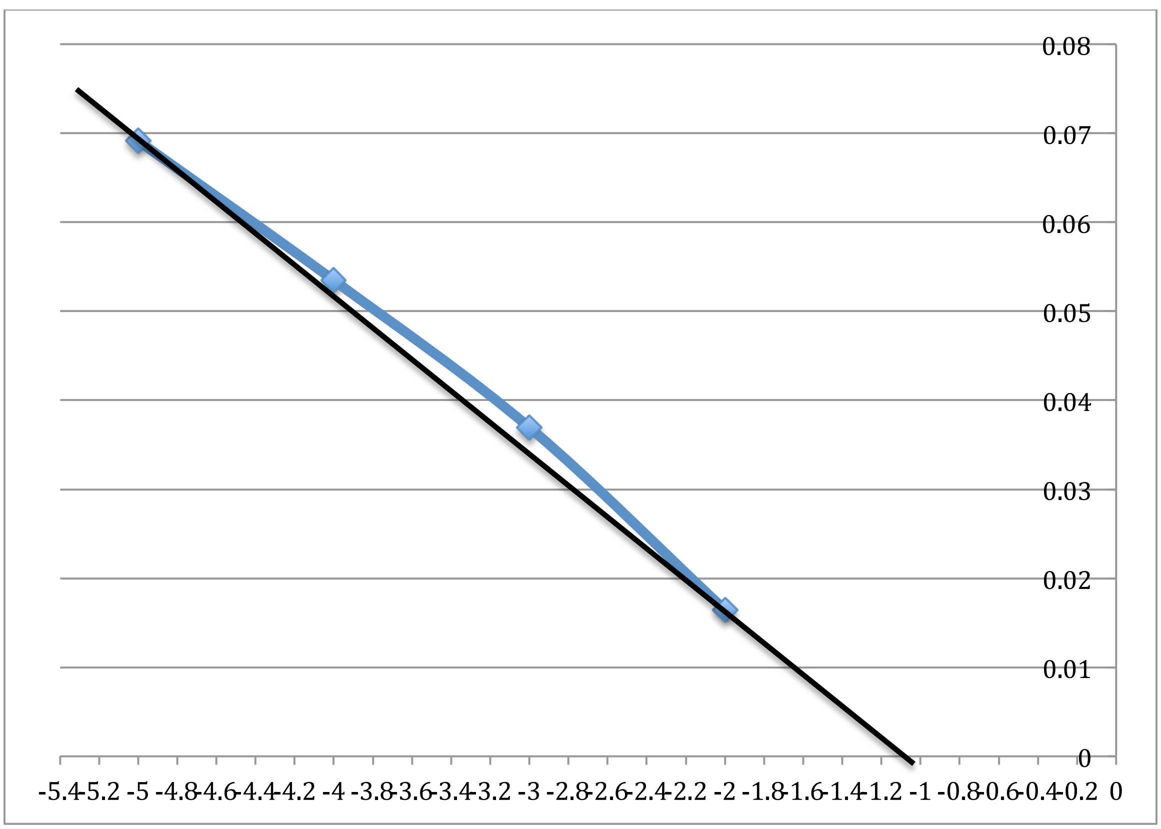
$\lambda p = 1/((41{,}907.6385 \times 0.002955838)-4))$

Hence, $\underline{\lambda p = 0.008342 V^{-1}}$

In order to obtain Vt for NMOS, we will need the current values at which Vds=Vgs,

i (Amps)	x = V (volts)	y= $\sqrt{(i/1+\lambda V)}$
-0.00000021148	- 1	0.00045796
-0.000273976	- 2	0.0164158
-0.0013998	- 3	0.036954
-0.002955838	-4	0.053482
-0.004981724	-5	0.069153

Plotting the values for x and y, we get,



Now make the best-fit line for the graph and wherever it intersects the x-axis is the threshold voltage. Here Vt= -1.1 V.

Calculating Kp:

Kp = $2s^2$, where s is the slope of the best-fit line.

From the graph, s= 0.02-0.01/-2.3-(-1.6) = -0.014285

Kp = $2(0.014285)^2 = 4.0812245 \times 10^{-4}$ A/V^2

Chapter 6: Conclusion and further Improvements:

Thus we have obtained correct results for the analysis of both MOSFETs.

Although initially I intended to analyze the voltage transfer characteristics of an inverter, due to unavailability of required accessories, it could be performed.

We can analyze an inverter using the same setup, but we will require 5 probes for it and the drains for the NMOS and PMOS needs to be shorted. We will also require extra cables in order to do so.

Also, I could not perform the analysis for different temperatures due the absence of an appropriate substrate on which the die could be pasted to perform this experiment.

For further analyses, the inverter can be tested for its voltage characteristics. Temperature component can be introduced, since there is a temperature control unit to provide temperatures ranging from -30C to 200C.

Before starting with these tests, the availability of all the required components and accessories needs to be checked.

References:

[1] http://www.home.agilent.com/agilent/home

[2] http://www.ti.com/lit/ds/symlink/cd4007ub.pdf

[3] http://www.home.agilent.com/agilent

[4] http://www.cascademicrotech.com/